REMARKS

This is in response to the Office Action dated October 27, 2006. Claims 1-2, 4-5, 7-9, 11-13, 15-17 and 19-20 are pending.

Claim 1 stands rejected under 35 U.S.C. Section 103(a) as being allegedly unpatentable over Anderson in view of Hayasaka. This Section 103(a) rejection is respectfully traversed for at least the following reasons.

Claim 1 as amended requires "at least two of the plurality of through electrodes are connected to one another to form a first high-current through electrode that is in communication with a power supply, at least another two of the plurality of through electrodes are connected to one another to form a second high-current through electrode that is in communication with ground, a particular signal-routing through electrode is formed of only one of the plurality of through electrodes; and at least one of the plurality of through electrodes is a non-contact through electrode which is electrically isolated from the chip." In other words, at least one of the through electrodes "electrically link[s]" the front surface of the chip to the back surface of the chip and is a "*non-contact through electrode which is electrically isolated from the chip.*" For example and without limitation, see the right-hand non-contact through electrode 19 in Fig. 3 of the instant application which is electrically isolated from the chip; see also non-contact through electrodes 19 in Figs. 8-9.

The cited art fails to disclose or suggest the aforesaid underlined and quoted feature of claim 1. In particular, both Anderson and Hayasaka fail to disclose or suggest a non-contact through electrode electrically linking the front surface of the chip to the back surface of the chip which is a "*non-contact through electrode which is electrically isolated from the chip*" as required by claim 1.

The Office Action relies on Hayasaka at col. 11, lines 13-16, which states "not every chip having the metal plugs 4 need be connected with its neighbor by means of the plugs . . . . that is, one or more of the chips may be formed with metal plugs only for the purpose of heat radiation." First, it is pointed out that this portion of Hayasaka only appears to describe that the chip is not connected with its neighbor via the metal plug. Therefore, this relates to the connection between a metal plug in one chip and another metal plug in the chip above or below. This portion of Hayasaka does not describe a non-contact through electrode that is electrically isolated from the chip.

The Office Action appears to argue that, based on Figs. 4-5, and col. 10, lines 20-25, of Hayasaka, that the metal plug is isolated from the chip portions surrounding the plug. However, claim 1 requires that the non-contact through electrode is electrically *isolated from the* ***chip***. Claim 1 does not recite "chip portions surrounding the plug." The metal plugs relied on by the Office action in Figs. 4-5 of Hayasaka are clearly in electrical contact with the chips through which they pass, as evidenced by col. 10, lines 35-40, which describes that the metal plugs 4 electrically connect through solder bumps . . . allowing the chips 1b and 1c to be connected. Thus, the metal plugs relied on by the Office Action to allegedly support the position that the metal plugs are electrically isolated from the chip are indeed *not* electrically isolated from the chips. Hayasaka teaches directly away from the invention of claim 1 in this respect.

Additionally, the metal plugs of Hayasaka are apparently formed only for the purpose of heat radiation and do not carry electrical current. Therefore, they would not be considered "electrodes" by one of ordinary skill in the art. The cited references fail to disclose or suggest a through "electrode" that is electrically isolated from the chip.

Accordingly, even the alleged combination of Anderson and Hayasaka (which applicant believes would be incorrect in any event) fails to disclose or suggest (1) a through electrode which *electrically links* the front surface of a chip to a back surface of a chip, *and* (2) the *same* through electrode is *electrically isolated* from the chip in which it is formed. Thus, the cited art fails to disclose or suggest the subject matter of claim 1.

Claim 7 requires that "at least one of the through electrodes is a non-contact through type electrode which is not electrically connected to the semiconductor chip in which it is formed." Moreover, claim 8 requires that "at least one of the through electrodes is a non-contact through electrode which is electrically isolated from the semiconductor chip in which it is formed." The cited art fails to disclose or suggest each of these features of claims 7 and 8, respectively.

Regarding claims 9, 11, 12, 13, 15-17, 19 and 20, the Office Action has used impermissible hindsight reasoning to arrive at the claimed inventions. The Office Action asserts that it is well known that a larger total cross section is used for a longer conduction path to reduce impedance. The Office Action then asserts that one skilled in the art would connect through electrodes in order to reduce impedance. This latter assertion is certainly based on impermissible hindsight reasoning. Anderson teaches reducing impedance by using a wide, thick wire at col. 3, lines 57-64. Assuming arguendo for the sake of argument only that one were to combine Anderson and Hayasaka, one skilled in the art wishing to reduce impedance would apply the teaching of Anderson and provide wider, thicker metal plugs. However, the pending claims call for through electrodes with substantially equal cross-sectional area, so this modification would not meet the pending claims. Moreover, Anderson teaches connecting a plurality of solder bumps in order to provide GND and VDD to various parts of the chips, the connection of multiple solder bumps in Anderson is entirely unrelated to reducing impedance;

impedance is reduced in Anderson by using wide, thick wires. Thus, the rationale alleged by the Examiner for the combination lacks merit and is fundamentally flawed. Stated another way, one of ordinary skill in the art would not have made the modification alleged at page 7, lines 7-14, in order to reduce impedance as alleged by the Office Action; instead, one would have reduced impedance by using wide, thick wires as taught by Anderson.

It is respectfully requested that all rejections be withdrawn. All claims are in condition for allowance. If any minor matter remains to be resolved, the Examiner is invited to telephone the undersigned with regard to the same.

Respectfully submitted,

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